REMARKS

This application is under final rejection. Applicant has presented arguments that Applicant believes should render the claims allowable. In the event, however, that the Examiner is not persuaded by Applicant's arguments, Applicant respectfully requests that the Examiner enter the arguments to clarify issues upon appeal. The status of the claims is as follows:

a. **Claims 1-10, 13-20** and **22-23** are **Pending** in the present application.

b. **Claims 1-10, 13-20** and **22-23** are rejected.

§102 Rejections

Claims 1-10, 13-20, 22 and 23

For ease of review, Applicant reproduces independent claims 1 and 13 herein below:

1. A method for forming a semiconductor device comprising:

forming a 3-dimensional (3D) pattern in a substrate; and

depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

13. A system for forming a semiconductor device comprising:

means for forming a 3-dimensional (3D) pattern in a substrate; and

means for depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

The Examiner states:

> **Claims 1-10, 13-20 and 22-23 are rejected under 35 USC §102(e) as being anticipated by Taussig et al. (US 6,861,365).**

Applicant respectfully disagrees. The present invention includes a method and system for forming a semiconductor device. Varying embodiments allow 2-dimensional alignment features to be created in 3-dimensional structures on a device substrate prior to any processing steps. Subsequent processing steps, including material deposition, planarization and anisotropic etching are utilized to construct a multi-level aligned pattern. Accordingly, the use of the method and system can potentially increase the flexibility of the semiconductor manufacturing process.

Claim 1 recites a method for forming a semiconductor device that includes forming a 3-dimensional (3D) pattern ***in a substrate*** and depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

The Examiner states that the Taussig reference anticipates the present invention. Applicant respectfully disagrees and asserts that ***the Taussig reference does not disclose forming a 3-dimensional (3D) pattern in a substrate as recited in claim 1 of the present invention***. (Emphasis added.) Taussig discloses a method and system for forming a semiconductor device. The method and system involves the utilization of a stamping tool to generate ***3-D resist structures*** whereby thin film patterning steps can be transferred ***to the resist*** in a single molding step and subsequently revealed in later processing steps.

Applicant argued in the response filed on October 23, 2006, that the Taussig reference does not disclose the formation of 3D patterns ***in a substrate*** as recited in claims 1 and 13 of the present invention. In response to this argument, the Examiner asserts that the Taussig reference clearly discloses in Figure 1 the step of forming a 3-D pattern (see step 130) in a substrate (see step 110) (also see col. 3, lines 14-30). Applicant respectfully disagrees. Col. 3, lines 14-30 read as follows:

> For a better understanding of the present invention please refer to FIG. 1. FIG. 1 is a high-level flow chart of the method in accordance with the present invention. First, a substrate is provided, via step 110. Preferably, the substrate comprises a flexible substrate adequate for use in a roll-to-roll fabrication process. Next, a layer of material is deposited over the substrate, via step 120. The material preferably comprises an organic or inorganic material. Finally, ***a 3-dimensional (3D) resist***

> ***structure is formed over the first layer of material wherein the 3D resist structure comprises a plurality of different vertical heights throughout the structure, via step 130***. Preferably, the 3D resist structure is generated by utilizing a stamping tool. Since the 3D resist structure comprises a plurality of different vertical heights throughout the structure, the structure can be utilized to transfer alignment patterns to an underlying layer based on subsequent etching steps. (Emphasis added.)

Applicant asserts that the Examiner is incorrectly correlating step 130 of the Taussig reference with the present invention of independent claims 1 and 13. Step 130 of Taussig discloses " a 3-dimensional (3D) resist structure is formed ***over*** the first layer of material wherein the 3D resist structure comprises a plurality of different vertical heights throughout the structure". (Emphasis added.) Applicant asserts that the first layer of material described in step 130 is the layer of material that was deposited ***over*** the substrate in step120. Consequently, the 3D pattern is formed in the layer of material that was deposited ***over*** the substrate and not the substrate as recited in independent claims 1 and 13.

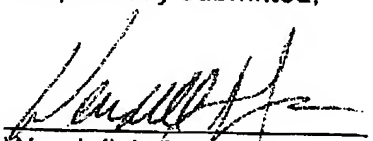
Applicant therefore asserts that Taussig discloses the formation of a 3-D pattern in a layer of resist material ***over*** a substrate and therefore clearly teaches away from the formation of a 3-D pattern ***in a*** substrate as recited in independent claims 1 and 13 of the present invention. Applicant accordingly asserts that the Taussig reference does not disclose every element of independent claims 1 and 13. Independent claims 1 and 13 are therefore patentably distinct in view of the Taussig reference and the rejections of claims 1 and 13 under 35 U.S.C. §102(e) ought to now be withdrawn.

Claims 2-10, 13-20 and 22-23

Since claims 2-10, 13-20 and 22-23 are respectively dependent on claims 1 and 13, the above-articulated arguments with regard to independent claims 1 and 13 apply with equal force to claims 2-10, 13-20 and 22-23. Accordingly, claims 2-10, 13-20 and 22-23 should be allowed over the Examiner's cited reference.

Applicant believes that this application is in condition for allowance. Accordingly, Applicant respectfully requests reconsideration, allowance and passage to issue of the claims as now presented. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,



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